

New Approach to Design and Implementation XOR Gate in QCA Technology

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Abstract

Quantum-dot cellular automata (QCA) is a novel technology that encodes binary information with state of electrons instead of voltage levels. QCA computations offer ultra-low power consumption, high speed and density construction. Majority voter and inverter are the most important gates in this technology and other gates and circuits can be implemented with them. In this paper, we design a novel fault tolerant two-input XOR gate. That is implemented in single layer without any wire crossing. One of the fundamental logical gates in digital circuits is exclusive-OR (XOR). Many circuits can be implemented with XOR such as full adder, comparator and so on. We design this gate according to Boolean expressions with one three-input majority gate and one five-input majority gate. The proposed design has significant improvement in terms of area, complexity, latency, and cell count in comparison to the previous designs. This component is suitable for designing fault tolerant QCA circuits. We simulate our design in QCA Designer and QCA Pro and achieved results are presented in this paper.

Keywords: Quantum-dot cellular automata (QCA). Exclusive-OR (XOR). Fault tolerant. Majority gate. QCA Designer. QCA Pro.

1. INTRODUCTION

Due to the challenge of increasing heat of chip in CMOS technology, researchers have to find new technologies [1, 2]. One of these technologies is quantum-dot cellular automata (QCA). It offers ultra-low-power consumption, small size, and also it works at THz frequencies. Several studies have reported that QCA can be used to design general purpose computational and memory circuits [3, 4]. It is suitable for parallel processing, as well. QCA offers a new method of computation and information transformation [5]. A QCA cell is the basic block in this technology. As mentioned, one of the fundamental logic gate in digital systems is XOR gate. It can be used in a wide

range for designing digital circuits. Meanwhile, defects and faults should be considered in QCA technology, circuits and gates should be fault tolerant.

In this paper, we propose a new fault tolerant design for XOR gate. The presented design is fault tolerant against cell omission and cell rotation defects. Simulation results show that the proposed design has significant improvement in decreasing latency, number of cells and increasing tolerance against defects and faults in QCA designs.

The paper is organized as follows. Section 2 gives the background of QCA by focusing on molecule and describing the type of defects; Sec

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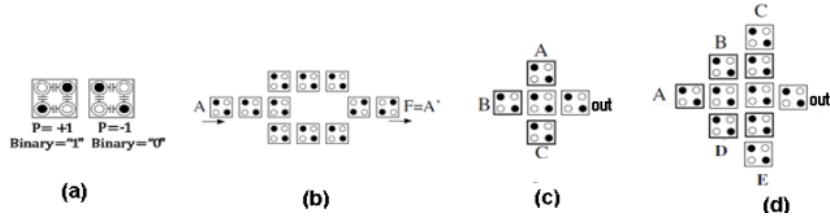


Fig. 1. (a) two possible polarizations, (b) inverter, (c) three-input majority voter, (d) five-input majority voter.

tion 3 explains the two new proposed designs for fault tolerant XOR gate; in Section 4 the methodology of designing XOR gate and the simulations set up are explained. In Section 5, we present the simulation results for power obtained from QCA Pro tool and finally Section 6 concludes the paper.

2. MATERIALS AND METHODS

2.1 QCA Background

Lent et al introduced QCA technology in 1993, it encodes binary information in charge of electrons instead of voltage level, because of that it has low-power consumption [2, 6, 7]. The basic element in this technology is cell. Each cell consists of 4 dots and 2 mobile electrons. These electrons are located according to Columbus Act, so, the cell have 2 possible polarization ($P=+1$, $P=-1$). Fig. 1a shows two possible polarizations. The polarization of each cell can be calculated [8, 9] as:

$$P = \frac{(p_1 + p_3) - (p_2 + p_4)}{p_1 + p_2 + p_3 + p_4} \quad (1)$$

The two polarizations can be binary either zero or one [1, 7, 10].

Majority voter and inverter are 2 basic gates in QCA technology, and other gates and circuits can be implemented by them [1, 11, 12], see Fig. 1b and Fig. 1c.

A three-input majority voter is implemented just with 5 QCA cells. In general, logical function of majority voter is,

$$M(A,B,C)=AB+AC+BC \quad (2)$$

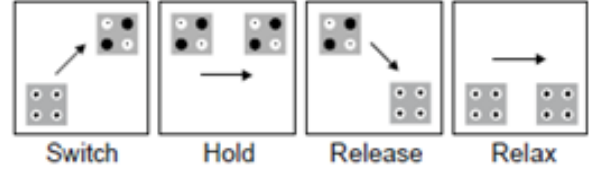


Fig. 2. Clock phases in QCA technology.

2.2 Five-Input Majority Gate

A five-input majority voter consist of five input and one output cells. Logical function of five-input majority voter is depicted in Eq. (3), where A, B, C, D, and E are inputs, (see Fig. 1d).

$$M(A,B,C,D,E)=ABC+ABD+ACD+ACE +ADE+BCD+BCE+BDE+CDE \quad (3)$$

2.3 QCA Clock

In this technology clocking technique is applied for signal flow and switching of QCA cells. Clock cycle consists of four phases: switching, holding, releasing, and relaxing. Fig. 2 shows the clock phases in QCA technology where each phase is shifted by 90° . In switching phase, cells are charging into one of two possible charge configurations. Data is latched in hold phase. In release and relax phases, the QCA cell is released and relaxed and electrons obtain mobility. Cells can be divided into different clock zones, so they have the same clock in a special zone [2, 4, 6, 7, 13, 14]. A cell latched in a clock and stay until the next clock leads it to the hold phase.

2.4 Fault and Defects in QCA

Defects are possible in deposition phase and synthesis phase in QCA [15]. Defects may occur in manufacturing procedure, generally are related to an individual cell. This type of defects involve in an extra or missing dot or electron in a cell. Other

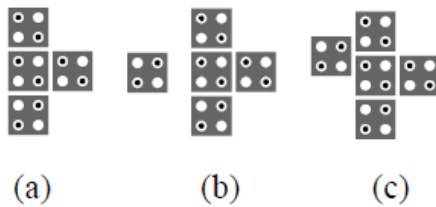


Fig. 3. Cell position defect in majority gate, (a) cell omission defect, (b) misplacement defect, (c) misalignment defect.

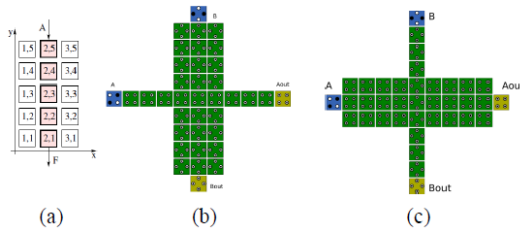


Fig. 4. Fault tolerant wires, (a) QCA fault tolerant wire [17], (b) thick horizontal cross over, (c) thick vertical cross over [18].

type of defects is for position of cells in QCA circuits. It includes misalignment, displacement and cell omission. When a cell is missed its direction, misalignment is happened. Misplacement is about misplacing the original place of a cell and missing a cell from its original position, results in cell omission defect [2, 7, 16]. Fig. 3 shows three types of cell position defects in a majority voter.

2.5 Fault Tolerant Gates and Circuits

Previous works generally have studied defect types and only a few numbers of them have offered fault tolerant QCA gates and circuits. Most fault tolerant models applied cell redundancy to resist cell position defects. Fault tolerant wire and crossover wire are shown in Fig. 4. Fig. 4a demonstrates QCA fault tolerant wire which employed three parallel conventional cell defects [17]. Two designs have been for fault tolerant coplanar crossover wire [18]. The design shown in Fig. 4b consists of a thick horizontal wire of normal cell and vertical normal wire of rotated cells while Fig. 4c shows other design in which a horizontal normal wire of cells is crossed to a vertical thick wire of rotated cells. In both designs, the thinner wire goes across the thick wire.

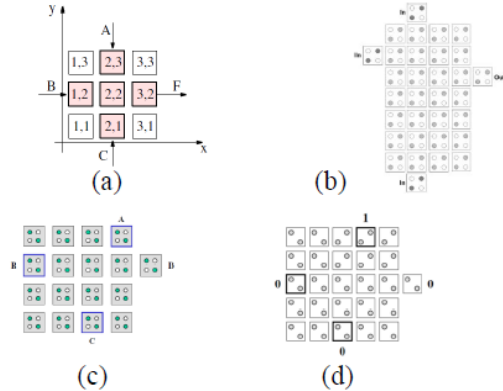


Fig. 5. Four types of majority voter a-d) references [17], [19], [20], [21] in order.

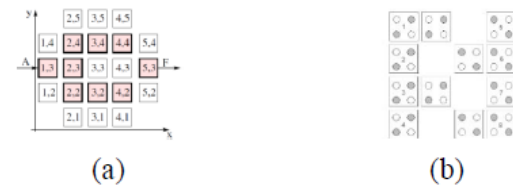


Fig. 6. QCA fault tolerant inverters (a-b) references [18] and [19].

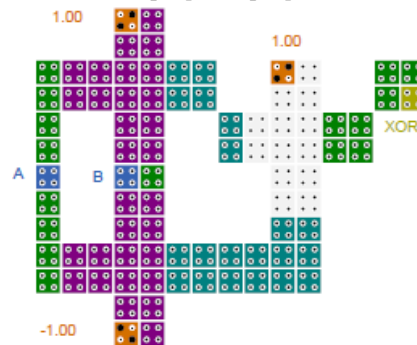


Fig.7. A fault tolerant 2-input XOR gate.

Fig. 5 shows four fault tolerant models for majority voter which are different in number of cells.

Two designs of fault tolerant inverter have also been introduced by [18] and [19]. Fig. 6 shows layout of fault tolerant inverters.

A fault tolerant 2-input XOR gate have been introduced in [22] that is shown in Fig. 7. This design uses 5 phases of clock cycle latency and does not have fan in.

2.6 Power Dissipation Analysis

The total energy of a QCA cell can be computed by using a Hamiltonian matrix. For an array of QCA cells, the Hamiltonian using Hartree-Fock

approximation and by regarding the columbic interaction between cells by a mean-field approach is expressed [23-25] as,

$$H = \begin{bmatrix} \frac{-E_k}{2} \sum_i C_i f_{i,j} & -\gamma \\ -\gamma & \frac{E_k}{2} \sum_i C_i f_{i,j} \end{bmatrix} \quad (4)$$

$$= \begin{bmatrix} \frac{-E_k}{2} (C_{j-1} + C_{j+1}) & -\gamma \\ -\gamma & \frac{E_k}{2} (C_{j-1} + C_{j+1}) \end{bmatrix}$$

Considering the similarly spaced neighboring cells, factor $f_{i,j}$ is absorbed into the Kink Energy definition (E_k). Kink Energy is associated with the energy cost of 2 cells (i.e. i and j) taking opposite polarizations and can be computed as [24],

$$E_{i,j} = \frac{1}{4\pi\epsilon_0\epsilon_r} \sum_{n=1}^4 \sum_{m=1}^4 \frac{q_{i,n}q_{j,m}}{|r_{i,n} - r_{j,m}|} \quad (5)$$

The expectation value for the energy of QCA cell at each clock cycle is obtained:

$$E = \langle H \rangle = \frac{\hbar}{2} \vec{\Gamma} \cdot \vec{\lambda} \quad (6)$$

where \hbar is reduced plank constant and $\vec{\Gamma}$ is the energy environment vector of the cell including its neighbor effects, and $\vec{\lambda}$ indicates the coherence vector. Eq.(7) gives Hamiltonian vector corresponding to Hamiltonian, where the term $(C_{j-1} + C_{j+1})$ is for the summation of neighboring polarizations,

$$\vec{\Gamma} = \frac{1}{\hbar} [-2\gamma, 0, E_k (C_{j-1} + C_{j+1})] \quad (7)$$

The power flows of a QCA cell are categorized into the four major flows P_{in} , P_{out} , P_{clock} and P_{diss} , where P_{in} and P_{out} flows are equal and P_{in} is the attained power from the left adjacent cell and P_{out} shows the released power to the right lateral cell. Overall the switch phase, inter-dot barriers are raised step by step leading toward transmission of a significant amount of energy to

the cell (P_{clock}) and during the release phase, the barriers are reduced regularly, therefor a deduction of this energy is returned to the clocking circuit. As a result, there is a trivial power dissipation called P_{diss} [26]. So, the instantaneous total power equation for a single QCA cell is,

$$P_t = \frac{dE}{dt} = \frac{\hbar}{2} \left[\frac{d\vec{\Gamma}}{dt} \cdot \vec{\lambda} \right] + \frac{\hbar}{2} \left[\vec{\Gamma} \cdot \frac{d\vec{\lambda}}{dt} \right] = P_1 + P_2 \quad (8)$$

where P_1 includes two main components: the first, power gain achieved from difference of the input and output signal power ($P_{in} - P_{out}$) and the second, transferred clocking power to the cell (P_{clock}) and P_2 represents dissipated power (P_{diss}) [25]. Based on [23]. The energy dissipation during one clock cycle $T_{\alpha} = [-T, T]$ can be represented in terms of Hamiltonian and coherence vectors,

$$E_{diss} = \frac{\hbar}{2} \int_{-T}^T \vec{\Gamma} \cdot \frac{d\vec{\lambda}}{dt} = \frac{\hbar}{2} \left\langle \left[\vec{\Gamma} \cdot \vec{\lambda} \right]_{-T}^T - \int_{-T}^T \vec{\lambda} \cdot \frac{d\vec{\Gamma}}{dt} \right\rangle \quad (9)$$

Maximum energy dissipation will occur when the changing rate of $\vec{\Gamma}$ is maximum. So by showing $\vec{\Gamma}_+$ and $\vec{\Gamma}_-$ as $\vec{\Gamma}(+T)$ and $\vec{\Gamma}(-T)$, the upper bound power dissipation model presented in [25] is given as,

$$P_{diss} = \frac{P_{diss}}{T_{cc}} < \frac{\hbar}{2} \vec{\Gamma}_+ \cdot \left[-\frac{\vec{\Gamma}}{|\vec{\Gamma}_+|} \tanh \left(\frac{\hbar |\vec{\Gamma}_+|}{K_B T} \right) + \frac{\vec{\Gamma}}{|\vec{\Gamma}_-|} \tanh \left(\frac{\hbar |\vec{\Gamma}_-|}{K_B T} \right) \right] \quad (10)$$

where T is temperature and K_B shows the Boltzmann constant. The total dissipated power can be calculated by adding the dissipated power of all cells since the presented model for each QCA cell is identical, in an array of similar QCA cells [18]. In [26], a power dissipation model for QCA circuits that separated the total power into two major parts which called "switching" and "leakage" were proposed. Leakage power is power

losses during clock changes (from low to high or high to low) and switching power is power loss due to the switching period leads to. Based on this model a power estimation tool called QCA pro [26].

3. PROPOSED FAULT TOLERANT XOR GATE

3.1 Preliminaries

As mentioned in previous section, XOR gate is one of the most important gate in logical circuits. The logical function for two-input XOR gate is obtained as,

$$x \oplus y = x'y + xy' \quad (11)$$

According to this function, we need 2 invertors and 3 majority gates to implement a two-input XOR gate. But it has different configuration and layout for implementing two-input XOR gate. Generally, there are two methods for implementing a XOR gate in QCA technology, 1- using wire crossing techniques that has more clock cycles which known as conventional approach, 2- using different algebra functions which needs less clock cycles but it does not have regular arrangement and flexible [1].

In [27] a property for five-input majority gate was introduced. As shown in Fig. 8, X, Y, Z are labeled as the main inputs and the control input is labeled control line and one of these inputs is twice as effective as other inputs on five-input majority gate. By setting the control line to "0", the Boolean function $(X(Y+Z))$ is obtained. In other hand, logical function $(X+YZ)$ can be achieved by changing the value of the control line into "1".

3.2 Proposed Two-Input XOR Gate

According to Boolean function introduced in previous section, set the control line to "0" logic value, the function will be,

$$M5(Y, X, X, Z, 0) = X(Y + Z) \quad (12)$$

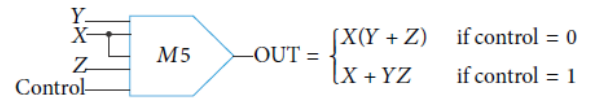


Fig. 8. Boolean function for five-input majority gate.

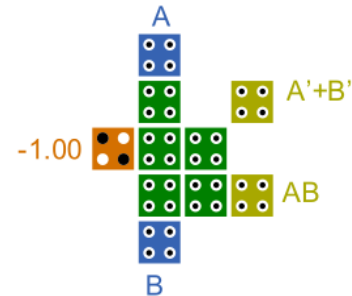


Fig. 9. Proposed three-input majority gate.

Considering A instead Y and B instead Z and $(A'+B')$ instead X, the XOR gate is,

$$M5(A, (A'+B'), (A'+B'), B, 0) \quad (13)$$

$$= (A'+B') + (A+B) = A' + B'$$

Accordingly, we need to have a three-input majority gate for presenting $A'+B'$ and also a five-input majority gate to implement a two-input XOR gate.

3.3 Proposed Three-Input Majority Gate

We use a three-input majority gate to achieve $A'+B'$. Fig. 9 shows our design for three-input majority gate whereas the inputs are A, B and the third is pushed to "0". So the majority gate convert to the AND gate and the output will be AB. In our design, we have (out) and (out') simultaneously so we have $A'+B'$ as well.

3.4 Proposed Five-Input Majority Gate

One of the basic methods to design fault tolerant gates in QCA technology is symmetric design. Also, in this paper, we got the idea to design five-input majority gate according to three-input majority gate. So we set QCA cells based on pointed two designs as shown in Fig. 10. It shows the five-input majority gate layout, where a, b, c, d and e are inputs and M is output.

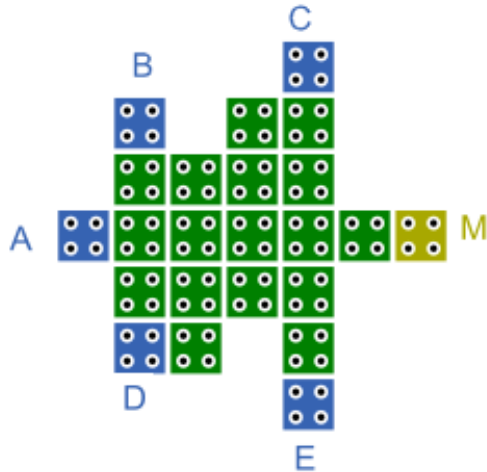


Fig. 10. Proposed five-input majority gate.

3.5 Proposed Fault Tolerant Two-Input XOR Gate

As mentioned in previous section, we use our proposed three-input and five-input majority gate by connecting them according to the previous description and giving proper clock to obtain two-input XOR gate. Fig. 11a shows the proposed two-input XOR gate, where ‘a’ and ‘b’ are inputs and XOR is the output. Cells marked as 1 and 2 shown in Fig. 11b are tolerant under cell omission and rotated cell defects.

3.6 Proposed Second Fault Tolerant Two-Input XOR Gate

To improve our proposed design, we used redundancy by adding some cells. The configuration is shown in Fig. 12.

This new XOR gate is more tolerant under cell omission and rotated cell defects. Fig. 13a-b

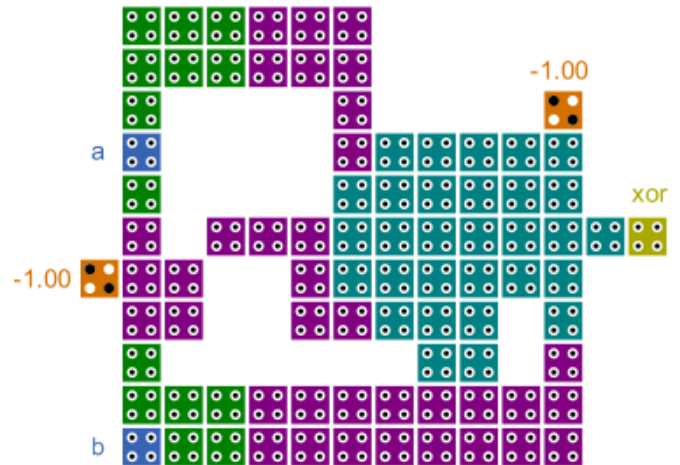


Fig. 12. QCA implementation for second proposed XOR.

shows that the cells can tolerate under cell omission defects and rotated cell defects respectively.

4. SIMULATION RESULTS

To verify the functional behavior of proposed XOR gates, we carried out simulations with bi-stable simulation engine of QCA Designer (version 2.0.3). The following parameters are used for a bistable approximation: cell size=18 nm, number of samples=50,000, radius of effect=65.000000nm, convergence tolerance=0.000010, clock high=9.800000e-023J, clock low=3.800000-023J, clock amplitude factor=2.000000, clock shift=0 and maximum iteration per sample=100. Most of the mentioned parameters are default values in QCA Designer. Simulation results for the proposed fault tolerant two-input XOR gates in Figs. 11-12 are shown in Fig. 14a-b respectively.

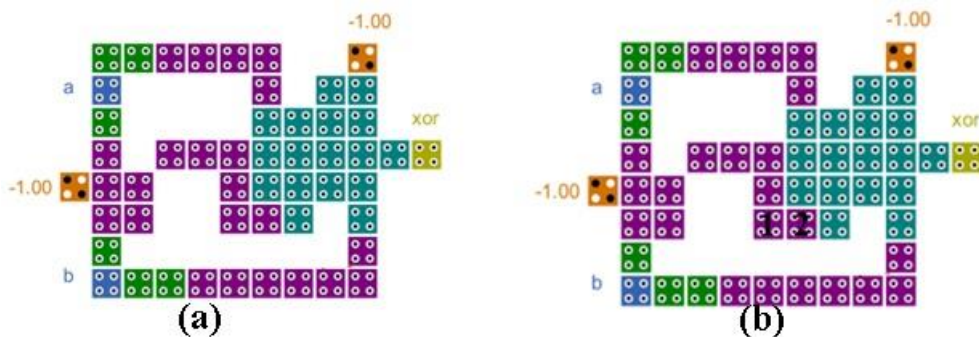


Fig. 11. (a) QCA XOR implementation, (b) cells can be tolerate under cell omission and rotated cell defects.

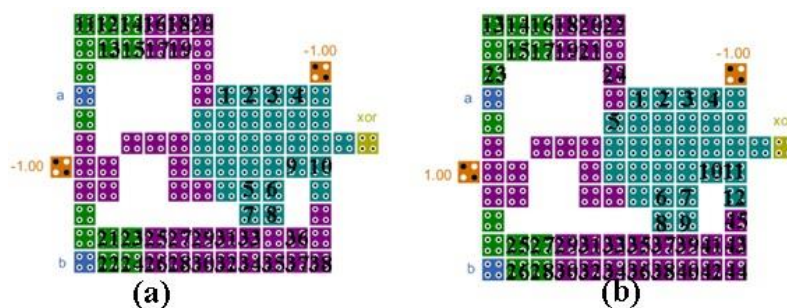


Fig. 13. (a) The cells can tolerate cell omission defects, (b) the cells can tolerate rotated cell defects.

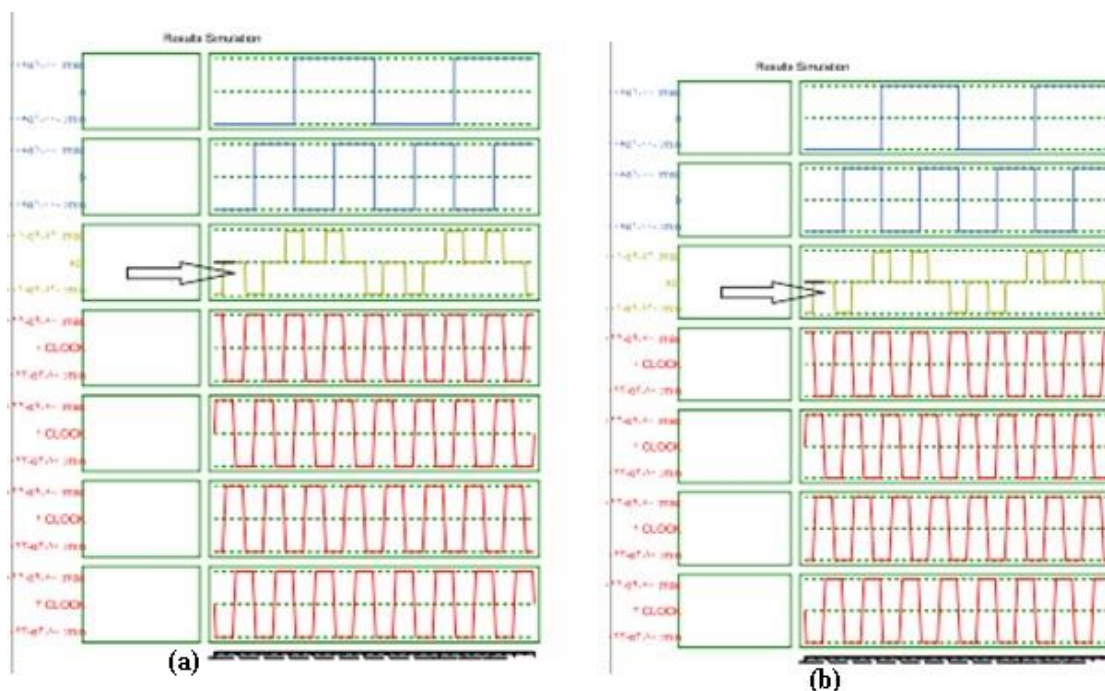


Fig. 14. Output result a-b) for Figs. 8-9.

According to Fig. 14, we can see that the correct output and also the strong polarization of the output cell for layouts. The start of each output signal is identified by an arrow on the figures. According to the results shown in Fig. 14a-b, we can get the correct output after 0/75 clock cycle.

Table 1 compares the previous works in two-input XOR gate with the proposed design in term Simulation results for the proposed fault tolerant two-input XOR gates in Figs. 11-12 are shown in Fig. 14a-b respectively. According to Fig. 14, we can see that the correct output and also the strong polarization of the output cell for layouts. The start of each output signal is identified by an arrow on the figures. According to the results

shown in Fig. 14a-b, we can get the correct output after 0/75 clock cycle. of hardware requirement and latency. According to Table 1 our designs do not have any cross over and they have 3 clock cycles latency that is the lowest delay for XOR gate. We used only 84 QCA cells which is the smallest area for fault tolerance XOR gates. Also, implementation in only one layer is important for fault tolerance designs.

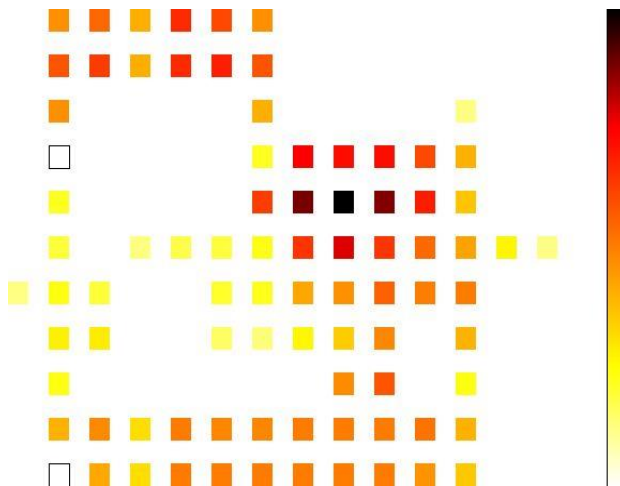
Furthermore Table 2 shows the percentage of fault tolerance against cell omission and rotated cell defects for the proposed XOR gates. Based on Table 2, about 50% cells in our design can be tolerate under cell omission and rotated cell defects.

Table 1. Comparison the previous works in two-input XOR gate deigns with the proposed XOR designs.

XOR structure	Cell count	Latency	Cross over	Fault tolerant	Fan in
Proposed design 1	51	3	No	Yes	Yes
Proposeddesign2	84	3	No	Yes	Yes
[22]	85	5	No	Yes	No
[28]	32	3	Multi-layer	No	Yes
[29]	62	6	No	No	Yes
[4]	42	3	Multi-layer	No	Yes
[13]	66	4	No	No	Yes
[14]	30	3	No	No	No
[30]	32	3	Multi-layer	No	Yes

Table 2. Percentage of cells can be tolerate under cell omission and rotated cell defects.

XOR gates	Percentage of cells can be tolerate under	
	Cell omission defect	Rotated cell defect
First proposed gate	3	3
Second proposed gate	45	53

**Fig. 15.** The power dissipation map for XOR gate at 2K temperature with 0.5 E_K design.

According to Table 1, it concludes that the result of proposed designs is significant improvements in number of cells, area and latency.

5. POWER RESULT

In order to evaluated the power consumption of our proposed method, we use QCA Pro [9, 31] as an acceptable power evaluator tool. The authors in [25] introduced a power dissipation model for QCA circuits. They categorized the total power into two major parts, called switching and leakage power and power loss per clock cycle at each cell due to switching power. We examine our design under three different tunneling energy levels (0.5EK, 1EK, 1.5EK) at 2K temperature. The power dissipation map of proposed XOR gate with 0.5 EK is shown in Fig. 15, where the high power dissipation cells are indicated using thermal hotspots with darker colors. The average leakage energy dissipation, average switching energy dissipation and average energy dissipation have been computed and written in Table 3. Based on Table 3, our XOR gate has normal power dissipation in different energy levels.

Table 3. Power results.

	Ave. leakage energy dissipation (meV)			Ave. switching energy dissipation (meV)			Ave. energy dissipation of circuit (meV)		
	0.5E _k	1E _k	1.5E _k	0.5E _k	1E _k	1.5E _k	0.5E _k	1E _k	1.5E _k
Proposed design	19.29	60.21	113.21	207.58	194.86	179.45	226.87	255.07	292.66
[22]	20.15	63.19	118.0	203.17	188.57	171.76	223.33	251.77	289.76

6. CONCLUSION

In this paper, we presented and simulated two new fault tolerant two-input XOR gates. First XOR gate had less number of cells and had less number of cells tolerate and the second design had more number of cells and also had more number of cells tolerate in terms of cell omission and rotated cell defects. Simulation was performed by bistable model in QCA Designer software. In these designs, we obtained accurate output values against defects. Energy dissipation results were performed by QCA Pro. Both of 2 gates were designed in single layer without any coplanar cross-over wiring. Simulation achievements approved that the proposed designing algorithm got significant improvement in terms of area, cell count, and latency.

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